AMENDMENTS TO THE CLAIMS

1. (currently amended) A ring oscillator comprising:

a plurality of delay cells coupled in series as a ring; and

a replica cell coupled to the delay cells to provide at least one bias signal to the delay cells, the replica cell including a differential transistor pair formed of a first transistor and a second transistor, the first transistor having a ~~drain~~ first terminal and a ~~gate~~ second terminal coupled to the ~~drain~~ first terminal, the second transistor having a ~~drain~~ first terminal and a ~~gate~~ second terminal coupled to the ~~drain~~ first terminal of the second transistor.

2. (currently amended) The ring oscillator of claim ~~1~~ 20, wherein the replica cell further includes:

a first active resistor connected between a power supply and the drain terminal of the first transistor; and

a second active resistor connected between the power supply and the drain terminal of the second transistor.

3. (original) The ring oscillator of claim 2, wherein:

the first active resistor includes a third transistor coupled in parallel with a fourth transistor that is diode-connected; and

the second active resistor includes a fifth transistor coupled in parallel with a sixth transistor that is diode-connected.

4. (original) The ring oscillator of claim 3, wherein the third, fourth, fifth and sixth transistors are PMOS transistors.

5. (original) The ring oscillator of claim 3, wherein the replica cell further includes an operational amplifier having:

an output coupled to respective gate terminals of the third and fifth transistors;

a first input coupled to a reference signal level; and

a second input coupled to the drain terminal of the first transistor.

6. (original) The ring oscillator of claim 5, wherein the replica cell further includes a current source connected to a tail of the differential transistor pair to provide a bias current for the differential transistor pair.

7. (original) The ring oscillator of claim 6, wherein the current source is a variable current source coupled to be controlled by an input signal for the ring oscillator.

8. (original) The ring oscillator of claim 7, wherein the output of the operational amplifier provides a bias signal level to active resistors of the delay cells.

9. (original) The ring oscillator of claim 8, wherein the input signal for the ring oscillator is coupled to control variable current sources of the delay cells.

10. (original) The ring oscillator of claim 9, wherein each of the delay cells includes a respective differential transistor pair coupled between respective active resistors of the delay cell and a respective variable current source of the delay cell.

11. (original) The ring oscillator of claim 1, wherein the first and second transistors are NMOS transistors.

12. (currently amended) A system comprising:

an optical transmitter circuit; and

a clock circuit coupled to the optical transmitter circuit;

wherein the clock circuit includes:

a first oscillator;

a first phase locked loop (PLL); and

a second PLL coupled between the first oscillator and the first PLL;

the second PLL including a ring oscillator, the ring oscillator including:

a plurality of delay cells coupled in series as a ring; and

a replica cell coupled to the delay cells to provide at least one bias signal to the delay cells, the replica cell including a differential transistor pair formed of a first transistor and a second transistor, the first transistor having a ~~drain~~ first terminal and a ~~gate~~ second terminal coupled to the ~~drain~~ first terminal, the second transistor having a ~~drain~~ first terminal and a ~~gate~~ second terminal coupled to the ~~drain~~ first terminal of the second transistor.

13. (currently amended) The system of claim ~~12~~ 21, wherein the replica cell further includes:

a first active resistor connected between a power supply and the drain terminal of the first transistor; and

a second active resistor connected between the power supply and the drain terminal of the second transistor.

14. (original) The system of claim 13, wherein:

the first active resistor includes a third transistor coupled in parallel with a fourth transistor that is diode-connected; and

the second active resistor includes a fifth transistor coupled in parallel with a sixth transistor that is diode-connected.

15. (original) The system of claim 14, wherein the replica cell further includes an operational amplifier having:

an output coupled to respective gate terminals of the third and fifth transistors;

a first input coupled to a reference signal level; and

a second input coupled to the drain terminal of the first transistor.

16. (original) The system of claim 15, wherein the replica cell further includes a current source connected to a tail of the differential transistor pair to provide a bias current for the differential transistor pair.

17. (currently amended) A method comprising:

providing a ring oscillator that includes a plurality of delay cells and a replica cell coupled to the delay cells to provide at least one bias signal to the delay cells, the replica cell including a differential transistor pair, ~~each transistor of the differential transistor pair having its drain terminal connected to its gate terminal,~~ the replica cell also including an operational amplifier, the operational amplifier having an inverting input coupled to ~~the drain~~ a terminal of one of the transistors of the differential transistor pair; and

applying a reference signal level to a non-inverting input of the operational amplifier to set a common mode output voltage of the ring oscillator.

18. (original) The method of claim 17, further comprising:

providing an output of the ring oscillator as an input to a phase locked loop.

19. (original) The method of claim 18, further comprising:

providing an output of the phase locked loop as a clock signal to an optical transmitter.

20. (new) The ring oscillator of claim 1, wherein:

the first terminal of the first transistor is a drain terminal and the second terminal of the first transistor is a gate terminal; and

the first terminal of the second transistor is a drain terminal and the second terminal of the second transistor is a gate terminal.

21. (new) The system of claim 12, wherein:

the first terminal of the first transistor is a drain terminal and the second terminal of the first transistor is a gate terminal; and

the first terminal of the second transistor is a drain terminal and the second terminal of the second transistor is a gate terminal.

22. (new) The method of claim 17, wherein:

each transistor of the differential transistor pair has a drain terminal and a gate terminal connected to the drain terminal of the respective transistor; and

the operational amplifier has an inverting input coupled to the drain terminal of one of the transistors of the differential transistor pair.